UNIT-V

DIGITAL SIGNAL PROCESSORS

PART-A

1) What is pipelining? what are the different stages in pipelining?

The pipelining refers to overlapping of execution of various phases of different instructions so that a number of instructions can be executed in parallel.

There are four stages in pipelining.

1. The fetch phase
2. The decode phase
3. Memory read phase
4. The execute phase

2) what is the function of parallel logic unit?

The parallel logic unit is a second logic unit that executes logic operations [AND, OR, XOR, etc] on data without affecting the content of accumulators.

3) write any two applications of DSP:-

1. Digital cell phones
2. Automated inspection
3. Video conferencing
4. Noise cancellation
5. Medical imaging
6. Satelite communication

4) How do a digital signal processor differ from other processor? what are the special features of digital signal processor?

The special features of digital signal processor

are

1. Fast data access
2. Fast computation
3. Numerical fidelity
4. Fast execution control

5. List the addressing modes of TMS 320C50 DSP processor:-

1. Direct addressing 2. Memory mapped register addressing 3. Indirect addressing 4. Immediate addressing 5. Dedicated-register addressing
6. Circular addressing.

6) Mention one important feature of Harvard architecture:-

The harvard architecture facilitate the simultaneous access of instruction and data in a single cycle. (ie). two memory access in one cycle.

7. what is an advantages of pipelining?

In processors without pipelining, the execution of instruction is performed one by one. (ie) after complete execution of an instruction the next instruction is fetched from memory.

In processor with pipelining, the instruction execution is divided into various phase/stage and execution of different phase of two or more instructions are performed in parallel.

So that computation time is less.

8. List the various registers used with ARAU:-

1. Eight Auxiliary registers (AR0-AR7)
2. Auxiliary register pointer
3. Unsigned 16-bit ALU.

9. What are the different Buses of TMS 320C54x processor and list their functions:-

1. Program Bus.
2. Program Address Bus.
3. Data read Bus.
4. Data read address Bus.

Function:-

1. The program bus carries the instruction code and immediate operand from program memory, to the CPU.
2. The program address bus provides address to program memory space for both read and write.
3. The data read bus interconnects various elements of the CPU to data memory space.
4. The data read address Bus provide the address to access the data memory space.

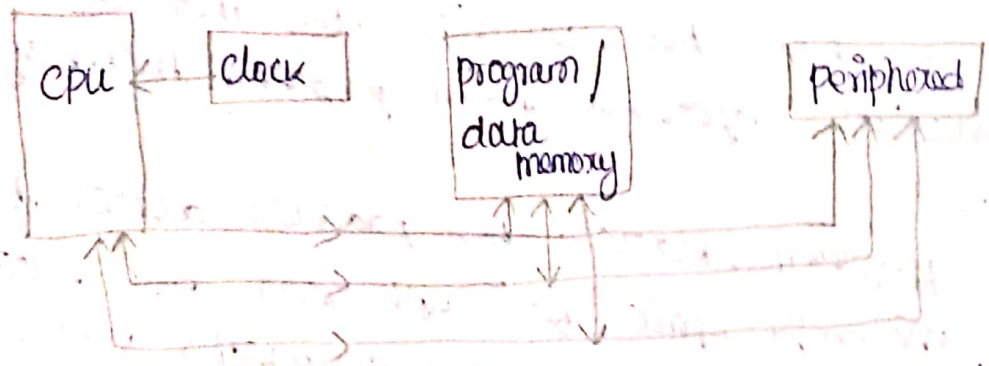
10. What is meant by memory mapped registers?

The TMS 320 C54x has 32 numbers of 16-bit CPU registers that are mapped into page-0 of data memory space. These memory mapped registers included registers for data and program memory address generation, various status and control registers for CPU and accumulators.

(1) Draw the block diagram of harvard architecture, Von neuman architecture and explain.

Von neuman Architecture:

In 1946, John Von Neuman developed the first computer architecture. In this, Instructions are stored in Read only memory (Rom). The Von Neuman Architecture is most widely used in majority of microprocessor.



In a computer with Von Neuman architecture, the CPU can be either reading an instruction or reading/ writing a data from/to the memory. Reading and writing can not access at the same time, since the instruction and data use the same signal pathways and memory.

The Von neuman architecture consists of three buses

1) The Data bus
2) Address bus
3) Control bus.

The Data bus:

Transport data between cpu and its peripherals.

It is bidirectional. The cpu can ~~be~~ read or write data in the peripherals.

The address bus:

The cpu user the address bus to indicate which peripherals it wants to access and within each peripheral which specific registers.

The address bus is unidirectional. The cpu always writes the address, which is read by the peripheral.

Control bus:

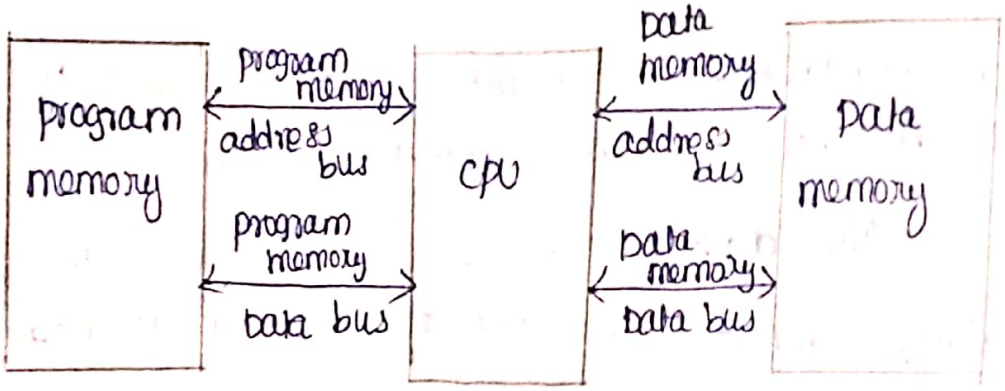
Control bus is responsible to synchronize the exchanges between the cpu and its peripherals, as well as that indicates if the cpu wants to read or write the peripherals.

Disadvantages of Von Neuman:

The main demerits of Von Neuman Architecture is that. It passes only one bus system. The same bus carries all the information exchanged between the cpu and the peripherals, including the instruction codes as well as the data processed by the cpu.

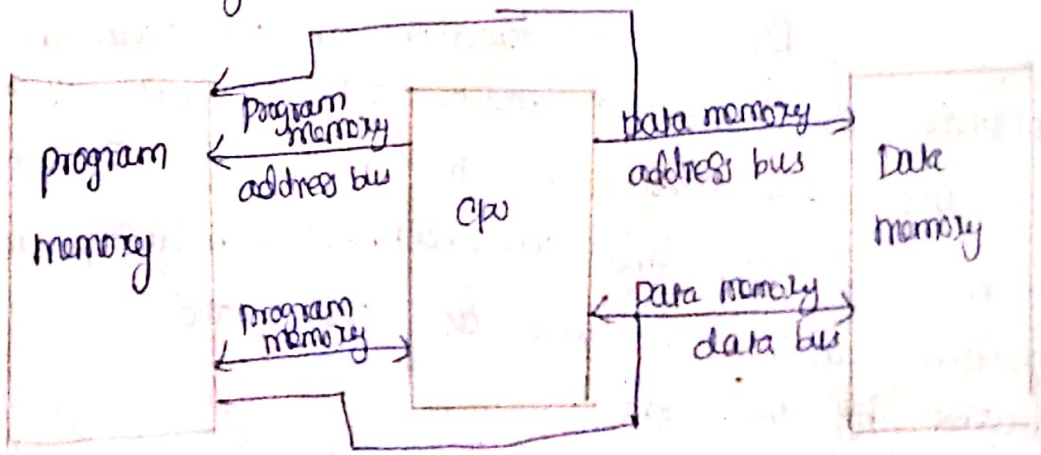
Harvard architecture:

The harvard architecture physically separates memories for their instructions and data, providing dedicated buses for each of them. Therefore instructions and operands can be fetched simultaneously.



Modified Harvard Architecture

In modified harvard architecture, one memory block is dedicated for storing data alone and another memory block for storing both instruction and data. This architecture will also have separate buses to access instruction and data simultaneously in one cycle.



Demerits:

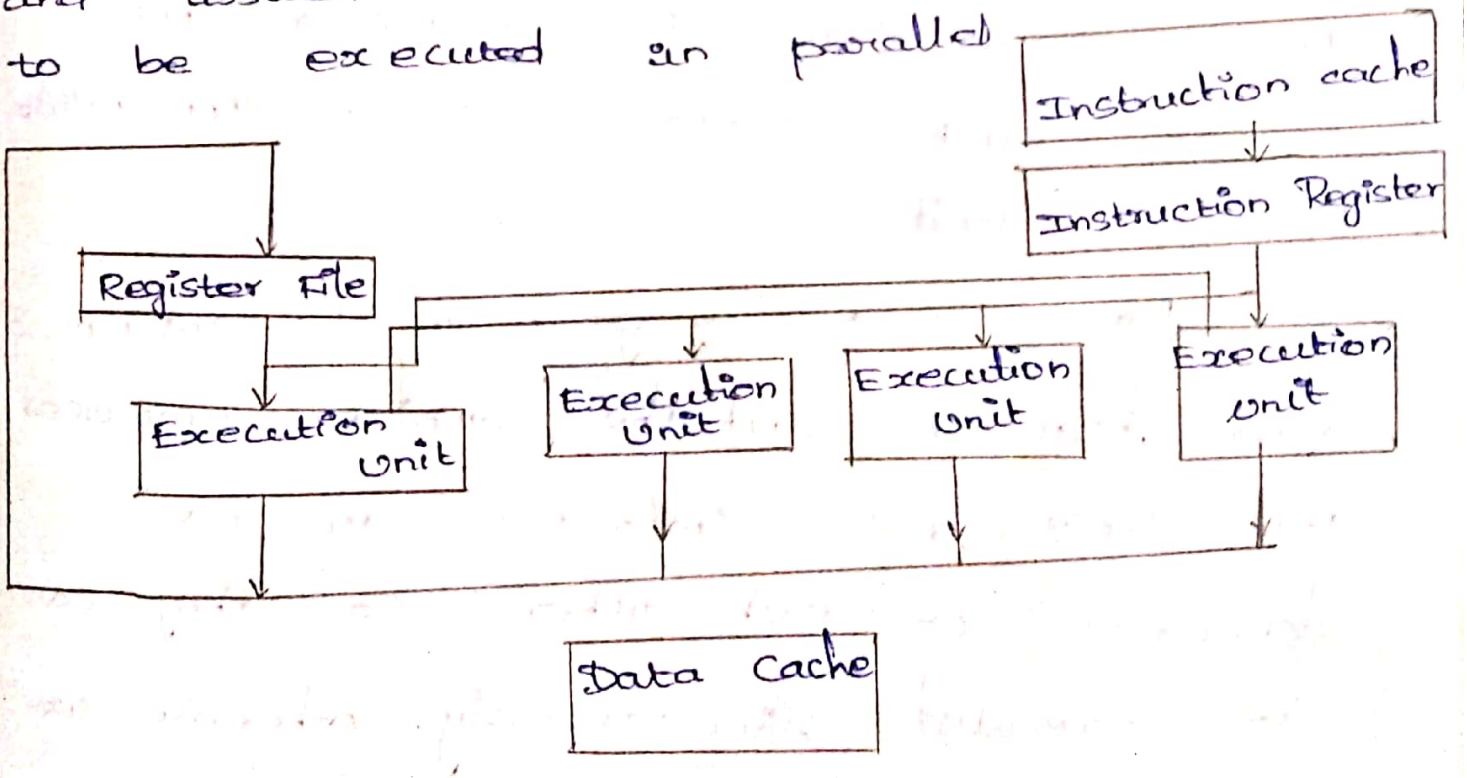
The modified harvard architecture uses separate bus system for program memory and data memory and inputs/outputs peripherals. It may also have multiple bus system. These multiple bus system increases the "complexity of the CPU".

Advantages:

It access several memory location simultaneously, There by increasing the data throughout between memory and etc.

2. Explain the advantages and disadvantages of VLIW architecture (Nov/DEC - 2012)

VLIW Means Very long Instruction Word. architecture. In this processor Many Instructions are followed at the same time and issued to multiple execution units to be executed in parallel



The VLIW processor consists of architecture that leads a relatively large group of instructions and execute them at same time.

The VLIW processor combines many simple instructions to a single long instruction word that uses different registers.

In VLIW, A language compiles or pre-processor separate the program instructions into basic operations that are performed by the processor in parallel.

These operations are placed into a "very long construction word" that the processor can then dix assemble & then transfer each operation to an appropriate execution unit.

For example, the group might contain four instructions and the compiler ensources that those four instructions are not dependent on each other so they can be executed simultaneously. otherwise it

places 'no-ops' (blams instruction) in the group where neccessary.

Advantages:

→ Increased performance.
→ Better compiler targets
→ potentially Scalable
→ Potentially easier to program.
→ can add more execution Units, allow more instruction to be packed.

Disadvantages:

→ New kind of programmer / compiler complexity
→ Program Must keep track of Instruction sheduling.
→ Increased Memory One
→ High power consumption
→ Misleading MIPS rating.

3. What is MAC Unit and pipelining. Explain its functions. MAC Unit [MAY / JUNE - 2014]

The fast computation is digital signal processor is achieved by MAC Unit [Multiply / Accumulate Unit]

The popular computation in digital signal processing are FFT, convolution & correlation. and Ge these operations involves multiplication and summation of laythy numerical arrays.

The MAC Unit in the CPU of digital signal processor is capable of computing one multiplication and addition in a single clock cycle.

Typically a MAC Unit will have a multiplier, a set of registers, a shifter and an ALU.

Example:

The instruction "MACD pgm, dmo"

will define that multiply the contents of program memory (pgm) and data memory (dma) specified by instruction and add to the sum of previous products in the accumulator with appropriate shift in an single class cycle.

Let us consider the output of fir filter is given by,

$$y(n) = \sum_{k=0}^{N-1} x(k)\,h(n-k)$$

In the above equation to compute the output, the minimum requirement is to Quickly multiply two values and also add the result. To make it possible, a fast dedicated hardware. MAC. Using either fixed-point or floating point arithmetic is mandatory.

Typical fixed point MAC Include

1. 16x16 bit 2's complement inputs
2. 16x16 bit Multiplies with 32-bit produces in 25ns
3. 32/40 bit accumulator.

1 MAC Functions:

A MAC Unit performs the following

→ Reads a 16-bit sample data.

→ Increment the sample data pointer by 2.

→ Reads a 16-bit co-efficient.

→ Increment the co-efficient sw register pointer by 2.

→ Sign multiply (16-bit) data and co-efficient to yield a 32 bit result.

→ Adds the result to contents of a 32 bit register pair for accumulate.

The TMS 320 C54x multiply, accumulate Unit performs a 16 x 16 → 32 bit fractional multiply-accumulate operation in a single instruction cycle.

The multiplies supports signed/signed

Multiplication, signed / unsigned multiplication, and unsigned / unsigned multiplication.

Many instruction using the MAC unit can optionally specific automatic round to nearest rounding

Pipelining.

The pipelining refers to overlapping of execution of various phases of different instruction so that a number of instructions can be executed in parallel.

In DSP's the execution of each instruction is divided in 4 or 6 phases. In 4-phase pipelining, when first instruction in 4th phase of execution, the second will be in 3rd phase, the third will be in 2nd phase and fourth will be in 1st phase of execution

The steps in the pipelining are often called stages The basic action of any microprocessor can be broken down into a series of four simple steps. They are

1. The Fetch
2. The decode
3. Memory read
4. Execution

Fetching:

In which the next instruction is fetched from the address stored in the program counter

Decoding:

In which the instruction in the instruction register is decoded and the address in the program counter is incremented

Memory Read:

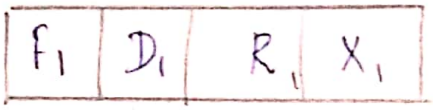
It reads the data from the data buses and also writes the data to the data buses

Execution.

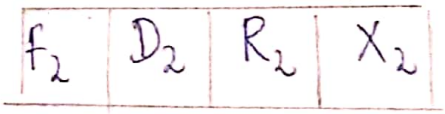
This phase execute the instruction currently in the instruction register and also completes the write process

Each of the above stages may be carried out seperately by four functional units

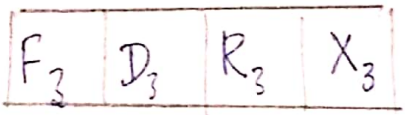
Instruction 1



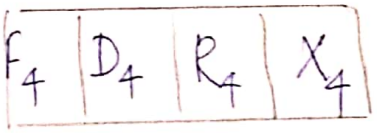
Instruction 2



Instruction 3



Instruction 4



Pipelining leads to dramatic improvements in system performance. The more pipelining stages, we can get more speed

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4. Explain Various Addressing modes of a digital Signal Processors. NOV/DEC 2011

ADDRESSING MODES:

The Addressing mode is the method of specifying the data to be operated by an instruction. The DSP processors support the following Six addressing modes

1. Direct Addressing
2. Memory Mapped registes Addressing
3. Indirect Addressing
4. Immediate Addressing
5. Dedicated Register Addressing
6. Circular Addressing

Direct Addressing.

In direct addressing, the lower 7 bits of data memory address are specified directly in the instruction itself. The upper 9 bits of the address will be the content of data memory page pointer (DP) is status register

Example:

ADDC 2ch [Add the content of data memory whose address is specified in the instruction

Memory Mapped Registe Addressing.

In memory-mapped register addressing the address of the memory-mapped register can be

Specified as direct address in the instruction

EXAMPLE:

LAMM 16h [Load accumulater with the content of memory mapped to address 0016h]

Reversed Addressing:

It is a special case of indirect addressing. In bit reversed addressing, the data memory address is specified by AR like indirect addressing, but the content of AR is incremented or decremented in order to generate the data memory address in the bit reversed order, using the content of index register.

EXAMPLE:

MAC 14F0h, * BR0 + [It defines as multiply the content of program(14F0h) by the data memory

Here the data memory is the content of AR currently pointed by ARP. The AR is incremented to generate the bit reversed addressed of data memory.

operand.

IMMEDIATE ADDRESSING:

In indirect addressing mode, the data memory address is specified by the content of one of the eight auxiliary register ($AR_0 - AR_7$). The AR currently used for accessing data is denoted by ARP [Auxiliary Register pointer]

Example:

LACC * , 0 ; Load the content of data memory addressed by AR , AR is not altered

LACC * +, 0 : Same as above , but AR is incremented by one.

LACC * -, 0 ; Same as above, but AR is decremented by one

SYNTAX USED IN INDIRECT ADDRESS FOR MODIFYING AR:

Syntax	Modification of AR
*	AR Unaltered

*+	AR Incremented by one
*-	AR. decremented by one
*0+	AR Incremented by the content of Index Register
*0-	AR Decremented by the content of Index Registers
*BR0+	AR Incremented for bit reversed addressing using of index register

DEDICATED REGISTER ADDRESSING:

In dedicated register Addressing mode, the address of one of the operand is specified by a dedicated CPU Register BMAR [Block Move address register].

In another case of dedicated register addressing one of the operand is the content of a dedicated CPU register DBMR [Dynamic Bit Manipulation Register].

Example:

BLDD BMAR 6fh [The instruction will copy the content of source address to destination address]

The Source address is the content of BMAR. the lower 8 bits of destination address is 6Fh and upper 9 bits of destination address is the content of DP

CIRCULAR ADDRESSING:

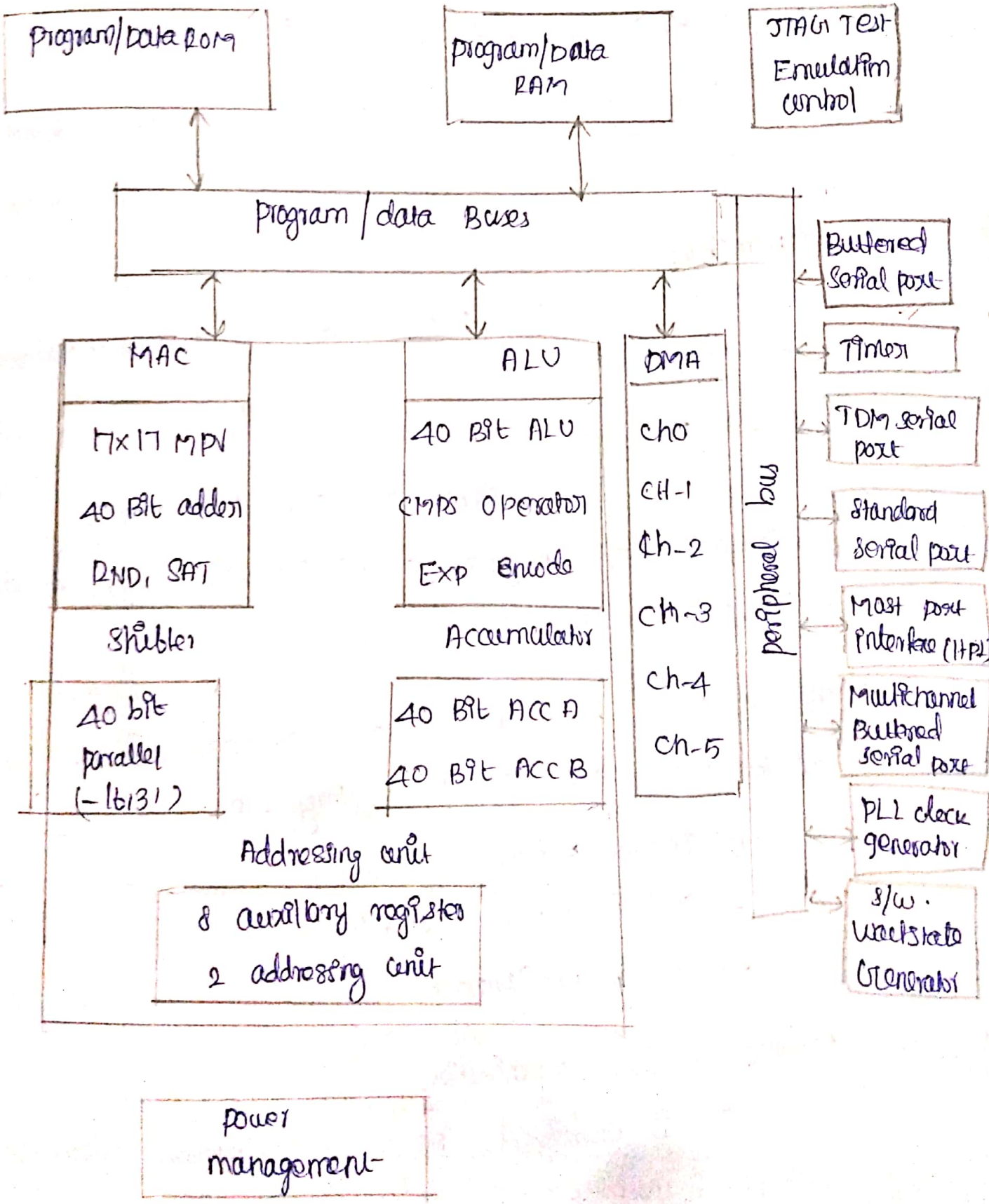
The circular addressing is similar to the indirect addressing. This addressing modes allows the specified memory buffer to be accessed sequently with a pointer that automatically wraps around to the beginning of the buffer when the last location is accessed

In order to hold the short and end addresses of the circular buffer. DSP Processor has four circular buffer register.

CBSR 1: Circular Buffer 1. Start Address Register
CBSR 2: Circular Buffer 2. Star Address Register
CBER 1: Circular Buffer 1. End Address Register
CBER 2: Circular Buffer 2. End Address Register

(5) With suitable block diagram explain in detail about TMS320C54 DSP processor memory architecture [NOV/DEC 2011 May/June 2014]

Architecture of TMS320C54



TMS320C54 is a 16 bit fixed point digital signal processor.

It is fabricated with an advanced modified harvard architecture that has one program memory bus, three data memory buses and four address buses.

Fastest processor family runs - 160 MHz with 1.6 volt

Lowest voltage family runs - 120 MHz with 1.5 volt

Program bus:

It carries the instruction code and immediate operands from program memory.

CB, DB and EB Buses

It interconnects the CPU & data address generation logic, program address generation logic, on chip peripherals and data memory.

The functional block diagram of TMS320C54 can be divided into four sub blocks. They are.

1) Internal memory organization
2) Central processing unit (CPU)
3) Onchip peripherals

Internal memory organisation

It is organized into three individually selectable spaces. They are

* Program
* Data
* I/O space

The CISA devices can contain the following

* Read only memory
* Random Access memory

The RAM can divided into three type

1) Dual Access RAM (DARAM)
2) Single Access RAM (SARAM)
3) Two way shared RAM

Read only memory (ROM)

* It is part of the program memory space and in some cases part of the data memory space
* On most devices, the ROM contains a boot loader that is useful for booting to faster onchip or external RAM

* Dual Access RAM (DARAM):

It is composed of several blocks. Each can be accessed twice per machine cycle.

The CPU and peripherals can read from and write to a DARAM memory address in the same cycle.

Single Access RAM (SARAM)

* It is composed of several blocks. Each block is accessible once per machine cycle for either a read or a write. It is always mapped in data space

Two way shared RAM:

The devices with multiple cpu cores include two way shared RAM blocks.

All the shared memory is program write protected or read only by the cpu only DMA (Direct memory access) controller can write to the shared memory.

2) central processing unit cpu:

It contains the following function

1) Multiply Accumulate (MAC)
2) Arithmetic Logic unit (ALU)
3) Shifters
4) Accumulators
5) Addressing unit

Multiply Accumulate (MAC)

The TMS320C54 include a 17 bit x 17 bit multiplier a dedicated 40 bit adder for non pipelined MAC operation.

The multiplier supports signal / signed multiplication and unsigned / ~~sign~~ multiplication. These operation allow efficient extended precision arithmetic

Arithmatic Logic Unit:

It is implemented a wide range of arithmatic and logical functions. most of which execute in a single clock cycle.

After operation is performed in ALU, the result is usually transferred to destination accmulator.

The ALU can also function as two separate 16 bit ALUs and perform two 16 bit operations simultaneously

ALU input constructed in two ways:

→ If 15 through 0 contain data memory operand then 31 through 16 contain zero or sign extended.

→ If 31 through 16 contain data memory operand then 15 through 0 contain zero and 31 through 32 contain either zero or sign extended

Overflow Handling:

If ovm (overflow mode) = 0, the accumulators are loaded with the ALU result without modification.

If ovm = 1 the accumulator are loaded with most positive 32 bit value or most negative 32 bit value depending on direction of overflow.

Shifters:

It can perform arithmatic & logical shifts by up to 31 bits left or by up to 16 bit right

Shifter i/p can come directly from data memory from either of two accumulator

Shifter o/p can be sent ALU or stored in memory.

Accumulators:

39 - 32	31-16	15 - 0
AG	AH	AL
Guard Bits	High order bits	low order bits

39-32	31-16	15-0
BG	AH	BL
Guard Bits	High order bits	low order bits

Accumulator A & B can be destination register for either the multiplier/adder unit or the ALU.

Each accumulator is spilt into three parts. The guard bits are used as a head margin for computations.

AG, AH, AL, BG, BH and BL are memory mapped register.

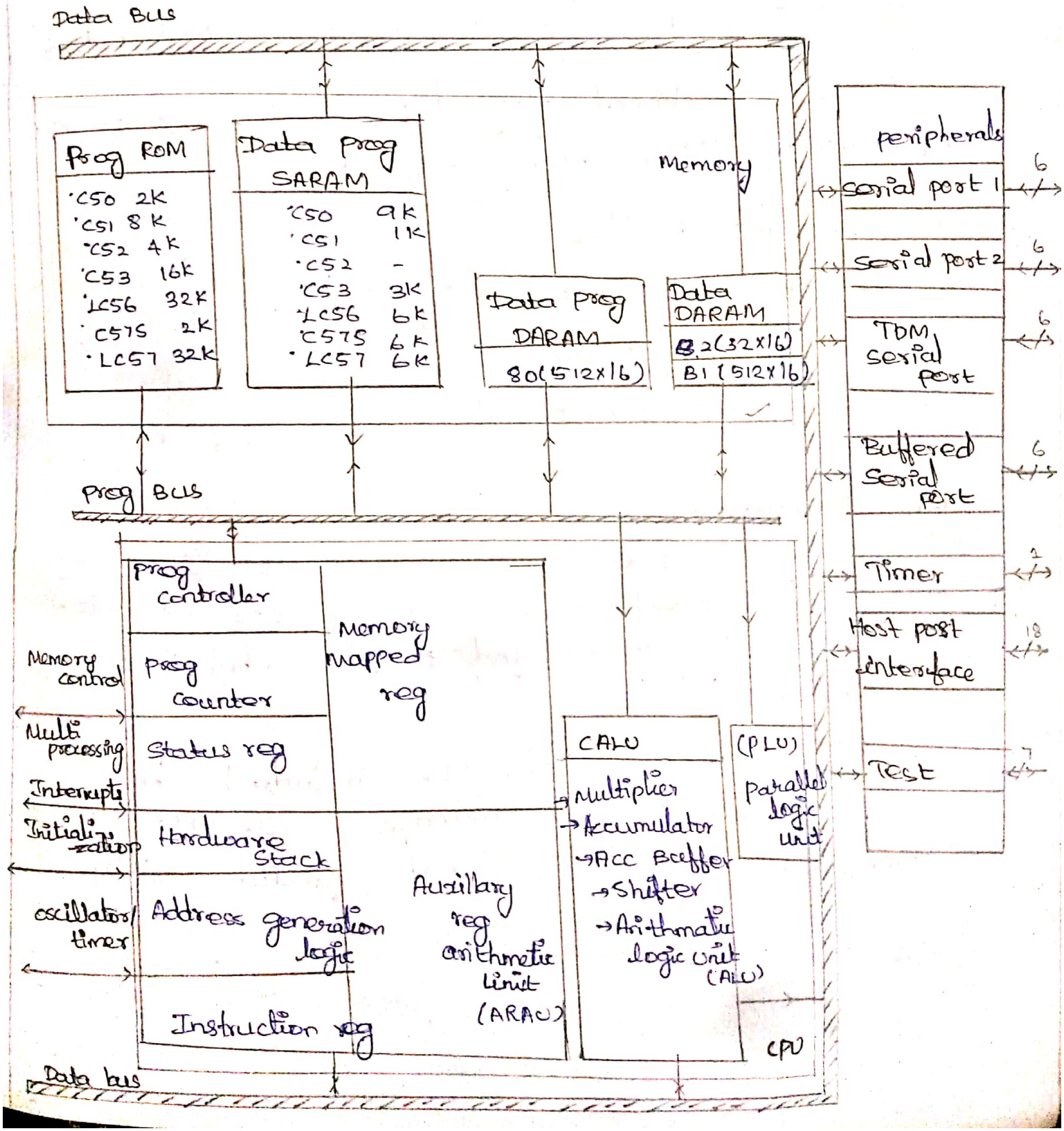
Addressing Unit:

The CSA DSP has three Status & logical registers: Status register 0, Status register 1 and processor mode Status

register (PMSR)

ST0 and ST1 contain the status of various condition and mode. PMSR contain memory setup status and control information.

6. Explain architecture of TMS320 C50 with neat dig [MAY / JUNE 2013, Nov / DEC - 2010]



TM320C50 digital signal processor is - fabricate With CMOS integrated ckt technology.

It is a fixed point 16 bit processor running at 40 MHz. The single instruction execution times is 50sec.

It's architectural design is based on combination of advanced Harvard architecture.

The functional block dig of TMS320C50 can be divided into four sub blocks.

→ Bus structure
→ CPU (central processing unit)
→ onchip Memory.
→ onchip peripherals

Bus structure:

Separate program & data buses in the advanced Harvard architecture of CSx maximize the processing power and provide a high degree of parallelism.

In addition the CSx included the control mechanism to manage interupts, repeated operations and function calling.

The C5x architecture has four buses:

- → Program Bus (PB)
- → Program Address Bus (PAB)
- → Data read address Bus (DAB)

⇒ Data read bus.

program Bus:

It carriers the instruction code and immediate operands from program memory of CPU.

program Address Bus:

It provides address to program memory space for both read and write.

Data read Bus:

It interconnect various element of CPU to data memory space.

Data read Address Bus:

It provides address to access the data memory space:

2) central processing Unit:

It consist of following elements,

- → central Arithmatic logic Unit (CALU)
- → Parallel logic Unit (PLU)
- → Auxillary Register Arithmatic Unit (ARAU)
- → Memory Mapped Register
- → program controller.

central Arithmetic Logic Unit :

The CPU uses the CALU to perform 2's Complement arithmetic. It contain of following:

- → 16 bit x 16 bit parallel multipler
- → 32 bit Acc buffer (ACCB)
- → product Register (PREG)
- → 32 bit accumulator (Acc)
- → Additional shiftors.

The 16 x16 bit hardware multiplier is capable of computing a signed or un signed 32 bit product in single machine cycle.

The product register holds the product.

The 32 bit ALU and accumulator implement a wide range of arithmatic & logic functions, the majority of which execute is cycle.

One i/p to ALU comes from accumulator and other i/p can be furnished from the product register to the accumulator buffer Multiplier.

(ACCB) or o/p of scaling shifter.

The result of operations performed in ALU stored in accumulator.

Parallel logic Unit: It is second logic unit that executes logic operations on data without affecting the contents of accumulators.

Auxillary Register Arithmatic Unit:

The C5x consists of register file containing eight auxillary register (AR0 - AR7) Each of 16 bit length, a 3 bit auxillary register pointer (ARP) and an unsigned 16 bit. ALU. The auxillary register file is connected to the auxillary register including those for CPU, serial port, timer and software Wait and state generator.

Program controller:

The program controller consist of logic circuitry that decodes the operational instructions, manages, the CPU pipeline, Stores the Status of CPU operations and

the conditional operations. It consist of following elements,

→ Program Counter
→ Status and control Registers.
→ Hardware stack
→ Address generation logic
→ Instruction register.

Program Counter:

The C5x has a 16 bit program Counter(PC) which contains the address of internal or external program memory used to fetch instructions.

status and control Registers:

The C5x has four status & control register. They are,

→ circular Buffer control Register
→ Process mode status Register
→ Status Register ST0 & ST1.

circular Buffer control Register:

The C5x control two Concurrent circular Buffers.

→ CBSR1 & CBSR2 - Indicats When circular Buffers Starts.

CBER1 & CBER2 - Indicates when circular buffer end.

Process mode status register:

It resides in memory mapped space of data memory page 0 and can be saved in same way other data memory location.

Status register STO & STI:

It can be stored into data memory & loaded from data memory.

Hardware stack:

It is used in during interrupts and subroutine to save & restore the pc contents.

Address generation logic:

The address for the program address bus is generated by the program counter when instruction & long immediate operands are accessed.

Instruction Register:

The 16 bit instruction register hold the opcode of the instruction being executed.

3) On chip Memory:

The C5x architecture has a total memory address range of 224K words x 16 bits. The memory space is divided into four memory segments

→ 64K Word - program memory space.

→ 64K Word - local data Memory space.

→ 64K Word - i/p / o/p ports

→ 32K Word - Global data Memory Space.

The large onchip Memory of C5x includes,

→ program read only Memory

→ Data/program single access RAM (SARAM)

→ Data/program dual access RAM (DARAM)

Program read only Memory:

→ The C5x DSP carry a 16 bit on chip maskable programmable ROM.

→ MP/MC is high for Microprocessor.

→ Mp/Mc is low for Microcomputer.

Data/ Program Singal Dual Access RAM:

It can be configured in three ways,

→ Data Memory

→ program Memory

→ Data and program Memory.

Data / Program Dual Access RAM :

It can be configured in below:-

→ Block 0 - Data and program memory

→ Block 1 and Block 2 - Data Memory.

4) onchip peripherals:-

clock generator:

When PLL option is selected, the cpu clock is multiplied by a specific factor and generators a low freqeency clock than that of cpu.

Hardware timer:

The timer is an onchip down counter that can be used to

perdiocally generate cpo interrupts.

software programmable wait state generators:

It can extend external bus cycles up to seven Machine cycles.

General purpose I/O pins:

The c5x has two general purpose pins that are software controlled.

BIO - Mointers peripheral device status.

XF - Signals to external devices via Software.

Parallel I/o ports:

The c5x has 64 k parallel I/o ports..

Serial port Interfaces:

It consists of three different types of serial ports. They are,

→ General purpose Serial port.
→ Time Division Multiplexed Serial port
→ Buffered Serial port.

Buffered Serial port:

It is available on C56 & C57 devices. It operates on either auto buffering or non buffering mode.

TDM Serial port:

It is implemented on the C50, C51, and C53 devices. It operates in either TDM or non TDM mode.

Host port Interface:

It is 8 bit parallel port used to interface a host device or host processor to the C5x.

User Markable interrupts:

The C5x has four external, maskable user interrupts that external devices can use to interrupt the processor.

Part-C

① Explain or illustrate some of the application oriented operation of TMS320C50 processor

The following section provides application oriented operation for

* Modem application
* Adaptive filtering
* Infinite impulse response (IIR) filter
* Dynamic programming

Modem application

* The CSX devices with their enhanced instruction set and reduced instruction cycle time are particularly effective in implementing encoding and decoding algorithms

* Teaches the circular addressing, repeat block and single cycle barrel shift reduce the execution time of such routines.

* The differential and convolutional encoder for a 9600 bit/second V.32 modem use trellis coding with 32 carrier states

* The data stream to be transmitted is divided into groups of four consecutive data bits.

* The first 2 bits in time Q_{1n} and Q_{2n} in each group are differentially encoded into Y_{1n} and Y_{2n} according to the following.

$$Y_{1n} = Q_{1n} + Y_{1n-1}$$

$$Y_{2n} = (Q_{1n} - Y_{1n-1}) \oplus Y_{2n-1} \oplus Q_{2n}$$

* This is done by subroutine diff.

* The two differentially encoded bits Y_{1n} and Y_{2n} are used as inputs to a conventional encoder subroutine ENCODE, which generates a redundant bit Y_{0n}. These five bits are packed into a single word by the PACK subroutine

Adaptive Filtering

* This is done by updating the coefficients as it is computationally expensive and time consuming.

* The MPYA, ZALR and RPTB instruction on the ex can reduce execution time

* Quantization error in the updated coefficients can be minimized if the result is obtained by rounding rather than truncating

* The RPTB (repeat block) instruction allows the block of instruction to be repeated without any penalty for looping

* The SARAM of the C5x can be modified in both the program and data spaces at the same time by setting the only and RAM control flags to 1.

* The coefficient table is located in SARAM. It is accessed by the MACD and MPY instruction without modifying an RAM configuration.

Infinite impulse response (IIR Filter)

The Nth order IIR filter is represented by the following two difference equations.

At time interval n

x(n) is the current input sample

y(n) is the output of the IIR filter

$$d(n) = x(n) - d(n-1)\,a_1 - \cdots - d(n-N+1)\,a_{N-1}$$

$$y(n) = d(n)b_0 + d(n-1)b_1 + \cdots + d(n-N+1)b_{N-1}$$

* The above equation is implemented on the C5x using the multiply-accumulate instruction (MAC, MACD, MADS, MADD)

* It also requires a data move operation to update the state variable sequence d(n)

Dynamic programming

* It is used in optimal search algorithms

* The application such as speech recognition, telecommunication and robotics used dynamic programming algorithms.

* Most realtime search algorithms used the basic dynamic programming principle that the final optimal path from the start state to the goal state always passes through an optimal path from the state to an intermediate state.

* Identifying intermediate paths reduces a long time consumption search to the final goal.

* An integral part of any optimal search scheme based on the dynamic programming principle is the backtracking operation.

* The backtracking operation is necessary to retrace the optimal path when goal is reached.

* The path history is stored in a circular buffer called each back tracking operation, the path history is updated by a search algorithm for the next time period.

* Each group of four consecutive memory location in the buffer corresponds to the expands of the four paths by one node.

* Each element of a group corresponds to one of the four states in that time period

② List out some of the application of TMS 320 DSPs?

Automotive

* Adaptive ride control
* Antiskid brakes
* Cellular telephones
* Digital radios
* Engine control
* Navigation and global positioning
* Vibration analysis
* Voice commands
* Anticollision radar

consumer:

* Digital radios/TVs
* Educational toys
* Music synthesizers
* pagers
* power tools

control:

* Disk drive control
* Laser print control
* Robotics control
* servo control
* Motor control
*

Graphics / Imaging

* 3D rotation
* Animation / digital maps
* Image compression
* Image enhancement
* pattern recognition

Industrial:

* Numeric control
* power line monitoring
* Robotics
* security access

Medical

* Diagnostic equipment
* Hearing aids
* ultra sound equipment

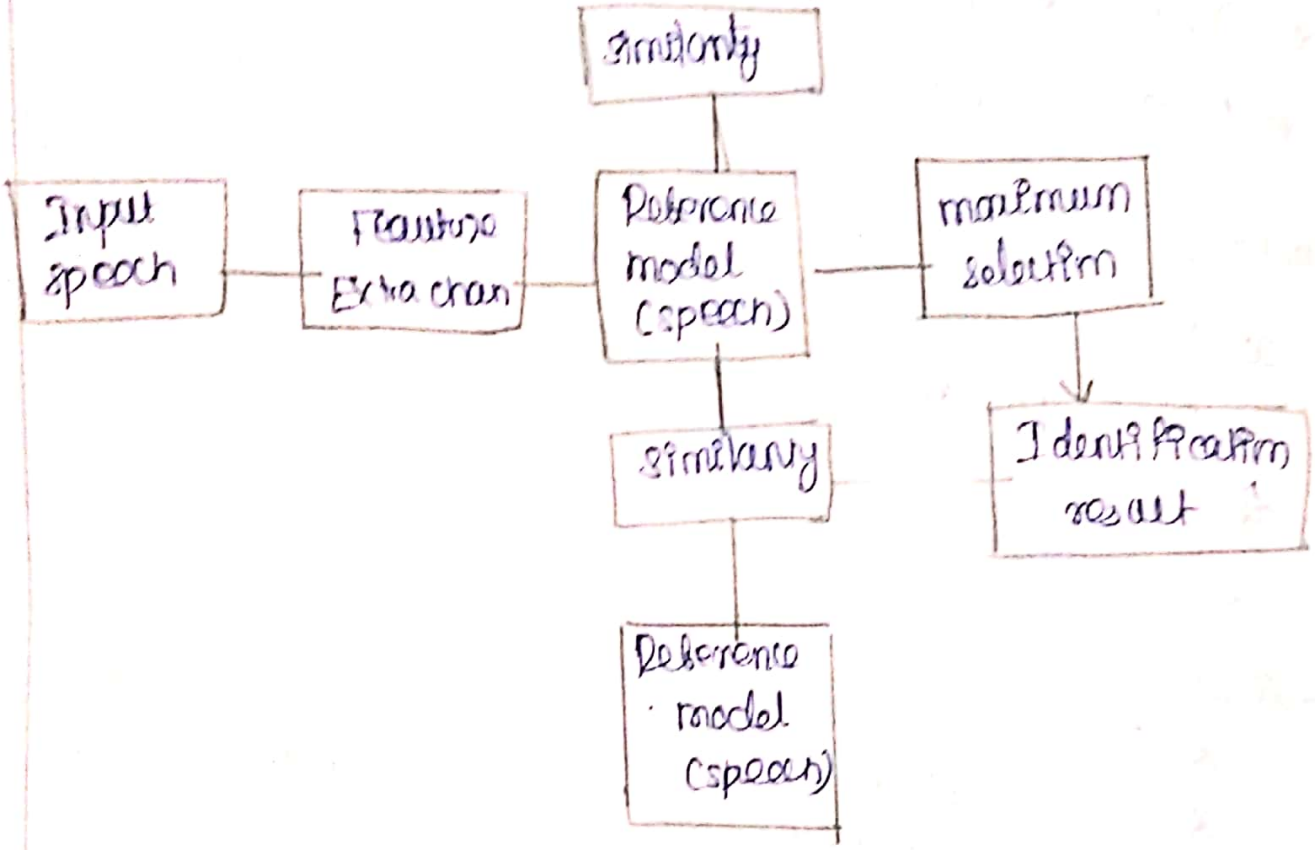
Military:

* Missile guidance
* Navigation
* Radar processing
* Radio frequency modems, sensor frequency

Voice speech

* Speaker verification
* speech enhancement
* voice mail

3) Design a device for speech recognition using DSP.



Feature extraction is the process that extracts a small amount of data from the voice signal that can later be used to represent each speaker.

Feature matching involves the actual procedure to identify the unknown speaker by comparing extracted features from his/her input utterance with those from a set of known speakers.

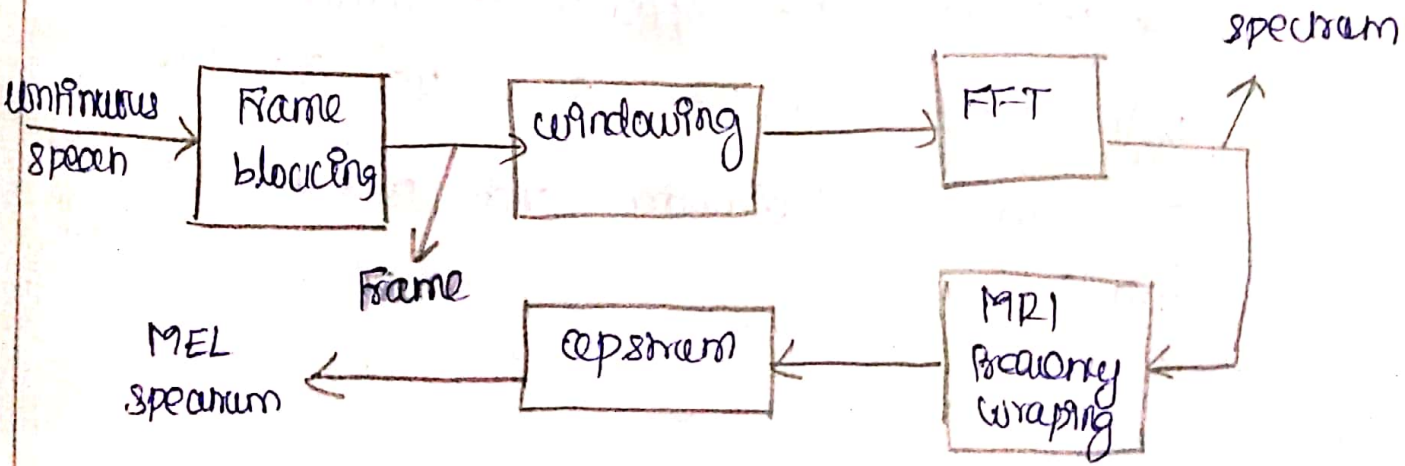
Speech Feature Extraction:

Convert the speech waveform to some type of parametric representation for further analysis and processing.

The speech signal is a slowly time varying signal.

MEL FREQUENCY CEPSTRUM COEFFICIENTS PROCESSOR

MFCC's are based on the known variation of the human ears critical bandwidths frequency filters spaced linearly at low frequencies and logarithmically at high frequencies have been used to capture the phonetically important characteristics of speech. The linear frequency spacing below 1000 Hz and a logarithmic spacing above 1000 Hz.



FRAME BLOCKING:

* Continuous speech signal is blocked into frames of N samples, with adjacent being separated by M. (M < N)

* The first frame consists of N samples second frame begins M samples after first frame and overlap it by M-N samples

* Third frame begins at 2M sample after first frames and it overlaps it by N-2M samples.

Windowing

* The next step in the processing is to window each individual frame so as to minimize. the signal discontinuities at the beginning and end of frame

* minimize the spectral distortion by using the window to alter the signal to zero at the beginning and end of each frame

Fast fourier transform:

* It converts each frame of N samples from the time domain into the frequency domain.
* The FFT is a fast algorithm implement the discrete fourier transform (DFT)

MEL Frequency wraping

The Mel frequency scale is linear frequency spacing below 1000 Hz and a logrithmic scale above 1000 Hz

capstrum:

* The log mel spectrum is converted back to time
* The result is called the mel frequency capstrum coefficients (MFCC)
* The capstrum representation of the speech spectrum provides a good representation of the local spectral properties of the signal

Feature ~~mechanism~~ Matching:

The feature matching techniques used in speaker recognition include dynamic time ~~wa~~ warping (DTW), hidden markov modelling (HMM) and vector quantization (VQ)