II year CSE / IV sem: EC8392 / Communication Engineering (19 copies)

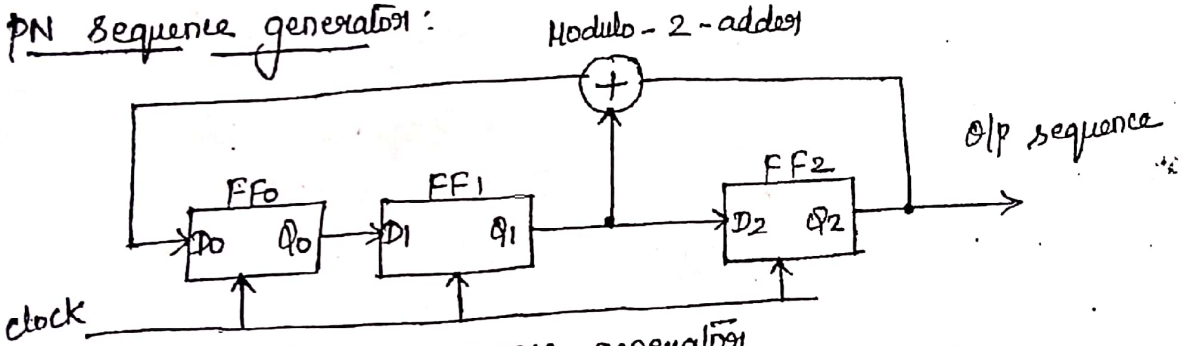
Unit-V Spread Spectrum and multiple access.

PN sequences, properties - m-sequence - DSSS - processing gain, Jamming - FHSS - synchronisation and tracking - Multiple access - FDMA, TDMA, CDMA.

PN sequences: is defined as "a periodic binary sequence with a noise like waveform that is usually generated by means of a feedback shift register (FSR). The same codes is used in both the transmitter and the receiver for a particular user for spreading and despreading.

→ It is also defined as a coded sequence of 1's and 0's with certain correlation properties.

PN sequence generator:



PN sequence generator

→ This is basically a shift register. Type D flip-flops are being connected such that the Q output of previous flip-flop is connected as input to D.

→ To obtain the PN sequence: Assume initial state of $Q_2Q_1Q_0$ ($Q_1Q_2Q_2$) to 100. The o/ps are connected to modulo-2 adder ie., an Ex-OR gate. The following table summarizes the operation of the PN generator.

→ A shift register of 'm' flip flops will have 2^m number of states, ie., $Q_0Q_1 \ldots Q_{m-1} = 000\ldots0$ to $Q_0Q_1 \ldots Q_{m-1} = 111\ldots1$. Thus the output will repeate itself after 2^m bits.

clock pulse number	Shift Register o/ps Q_2	Q_1	Q_0	Ex-OR gate o/p $Q_2 \oplus Q_1$	PN sequence Q_2	
0	0	0	1	$0 \oplus 0 = 0$	0	
1	0	1	0 ←	$0 \oplus 1 = 1$	0	
2	1	0	1 ←	$1 \oplus 0 = 1$	1	
3	0	1	1 ←	$0 \oplus 1 = 1$	0	
4	1	1	1 ←	$1 \oplus 1 = 0$	1	
5	1	1	0 ←	$1 \oplus 1 = 0$	1	
6	1	0	0 ←	$1 \oplus 0 = 1$	1	
7	0	0	1 ←	$0 \oplus 0 = 0$	0	The sequence repeats after this.
8	0	1	0 ←	$0 \oplus 1 = 1$	0	
9	1	0	1 ←	$1 \oplus 0 = 1$	1	
10	0	1	1 ←	$0 \oplus 1 = 1$	0	

→ The characters generated by a PN sequence generator depends on the number of flip-flops (m) used and on the selection of which flip-flops outputs are connected to the inputs of modulo-2 adder.

→ The state of each flip flop changes and gets shifted to the next flip-flops corresponding to each pulse of the clock.

→ The max. length of the sequence will be $2^m - 1$.

→ The duration of every bit in PN sequence is known as chip duration (T_c) and the chip rate (R_c) is defined as the number of bits (chips) / second.

$$R_c = 1/T_c$$

period of PN sequence $= T_b = NT_c$

(2) M-Sequence (or) maximal length sequence:

→ The maximum length sequence is a type of cyclic code which represents a commonly used periodic PN sequence.

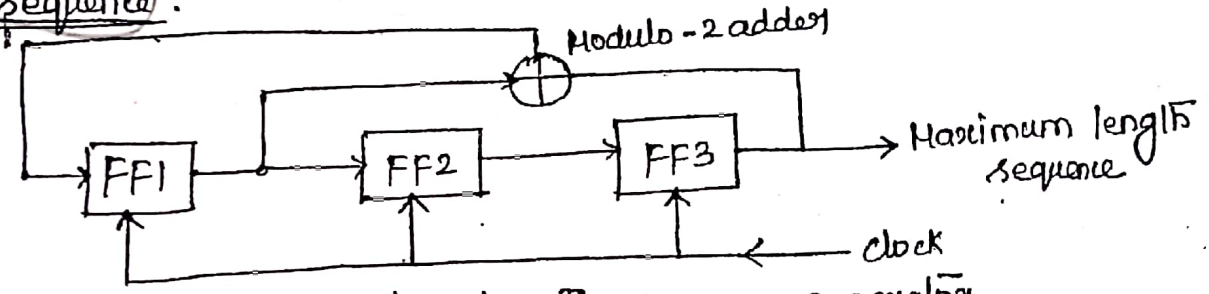
→ Such a sequence has long periods and requires a linear feedback Shift Register. A shift register of length 'm' consists 'm' flip flops and all of them operate on the same clock.

→ At each clock pulse, the state of each flip-flop is shifted to the next one. This input is computed by using a logical function of the states of all the flip-flops.

→ The maximum length sequence at the generator o/p will always periodic with a period of $N = 2^m - 1$.

m → Length of shift Register (or) number of flip flops.

→ The period of a PN sequence produced by a linear feedback shift register with 'm' flip-flops cannot exceed $2^m - 1$. when the period is exactly $2^m - 1$, then the PN sequence is called as m-sequence.

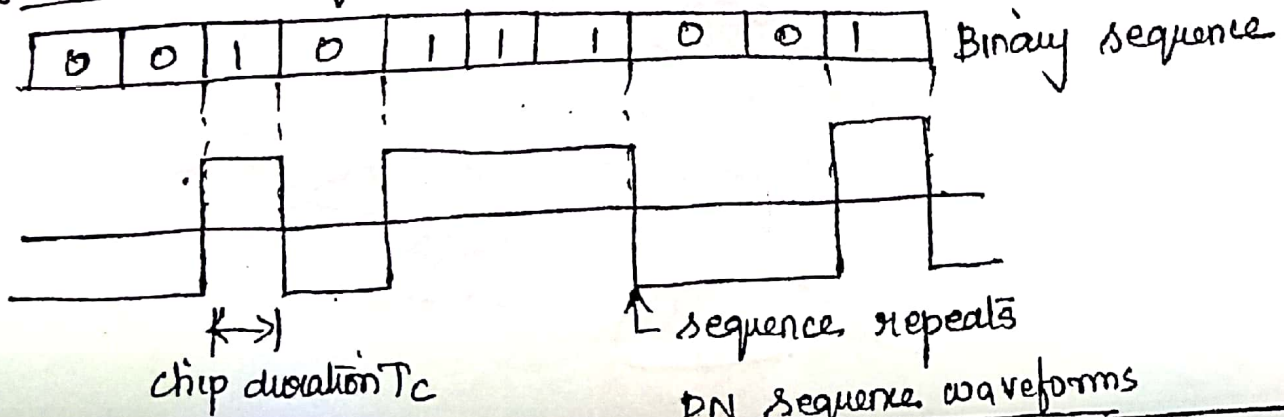


Maximum length sequence generator

→ A feedback shift register is said to be linear when the feedback logic consist entirely of modulo-2 adders.

→ If m=3, then the maximum length of the sequence is $N = 2^3 - 1 = 7$. The PN sequence repeats itself after every 7 clock cycles.

→ The PN sequence is an NRZ type signal with logic '1' represented by +1 and binary '0' represented by -1.



PN Sequence waveforms

properties of M-sequence:

The three properties are:

(i) Balance property: In each period of a maximal length sequence, the no. of 1s is always one more than the number of 0s. This called as balance property.

(ii) Correlation property: Auto correlation function of a maximal length sequence is periodic and binary valued.

(iii) Run property:

→ Run means a subsequence of identical symbols (1s or 0s) within one period of the sequence. Among the runs of 1's and 0's in each period of a maximal length sequence, one half the runs of each kind are of length one, one-fourth are of length two, one eight are of length three and ~~soon~~ so on.

→ For 'm' stage feedback shift register, the total number of runs will be $\frac{(m+1)}{2}$.

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④ Classification of spread spectrum (SS) Techniques.

SS modulation

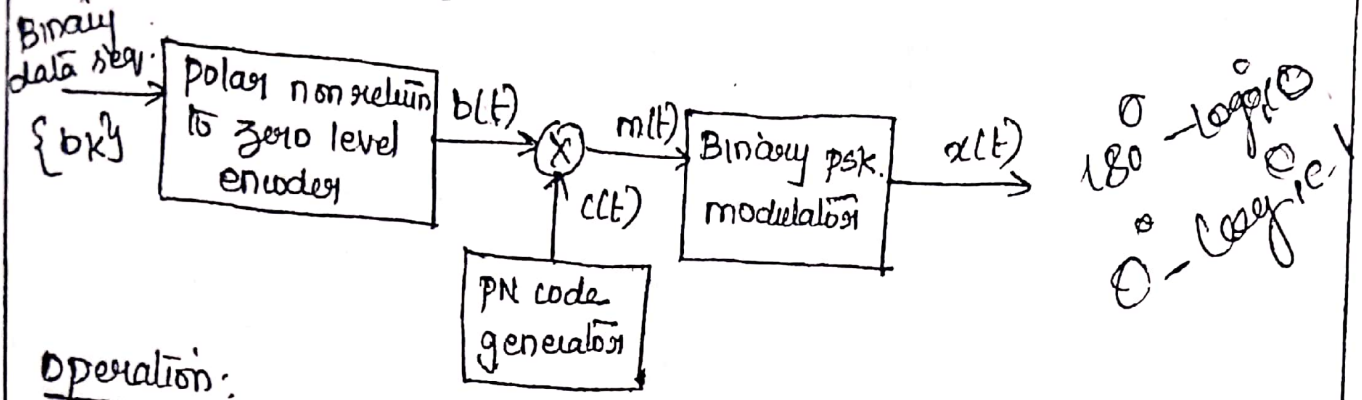
- Direct sequence spread spectrum (DS-SS)
- Frequency hop spread spectrum (FH-SS)

Direct sequence spread spectrum (DSSS)

→ In this DSSS technique, the I/p data sequence is used to modulate the pseudo-noise (PN) sequence directly.

→ Two stages of modulation are used. First, the incoming data sequence is used to modulate a PN sequence code (wide band). This code transforms the narrowband data sequence into a noise like wideband signal.

DS - BPSK Transmitter



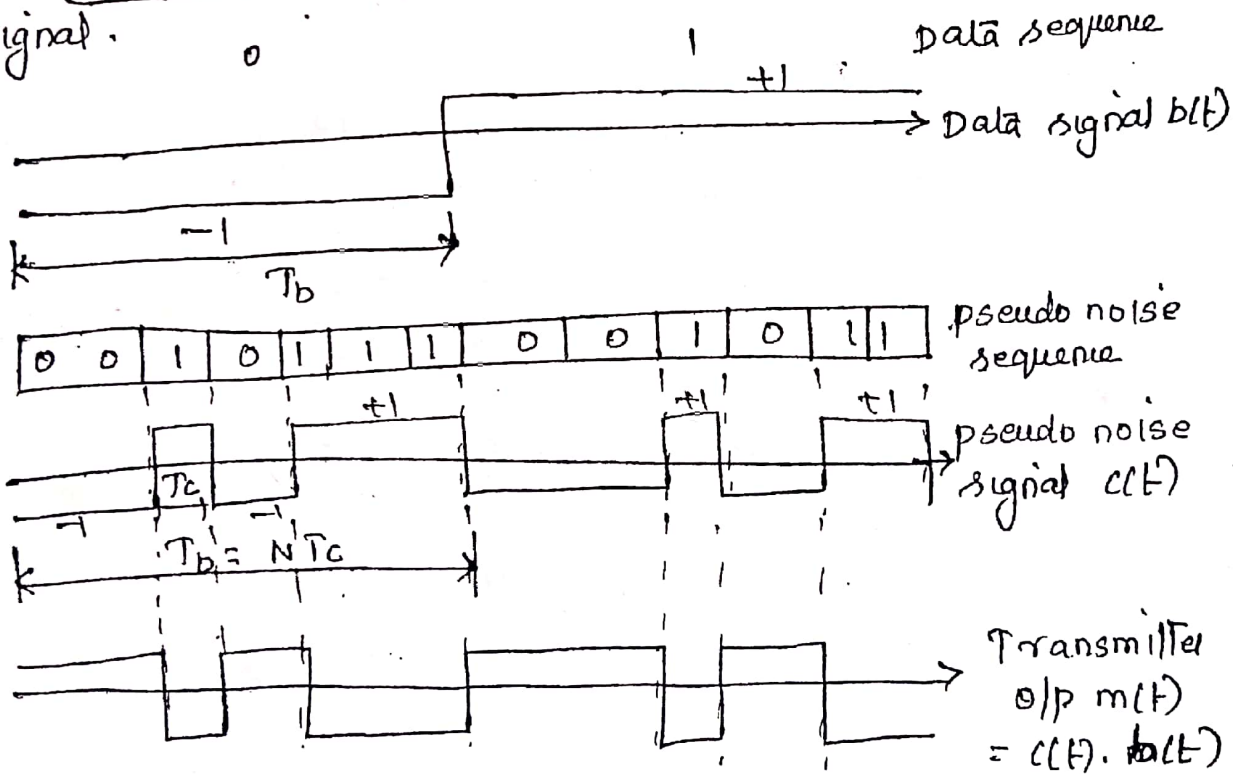
Operation:

→ The transmitter first converts incoming binary data sequence {bk} into a polar NRZ waveform b(t) by using NRZ encoder.

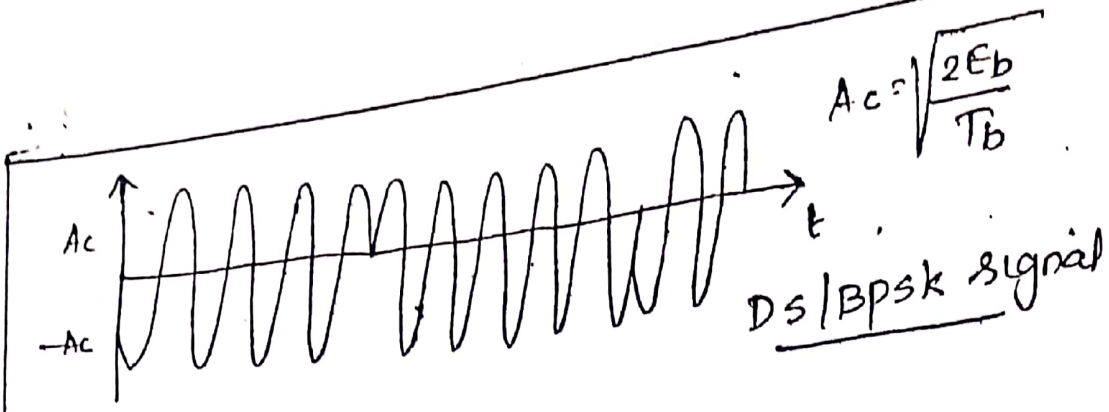
→ b(t) and PN signal c(t) from the PN-code generator are given as inputs to multiplier.

→ The o/p m(t) is modulated with BPSK modulation.

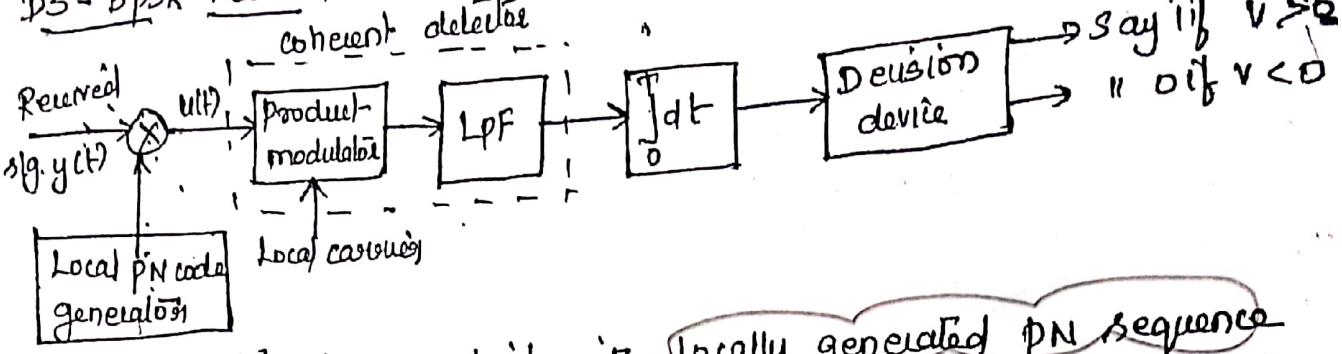
→ In the o/p signal x(t), phase 180° represents logic 0 and o/p phase 0° represents logic 1. The transmitted signal x(t) is a direct sequence spread binary phase shift keying (DS/BPSK) signal.



Transmitter o/p waveforms.



DS-Bpsk Receiver.



→ The multiplier is supplied with locally generated PN sequence which is an exact "replica" of the PN sequence used at the transmitter. The receiver needs to operate in perfect synchronization with the transmitter.

→ The received DS-Bpsk signal y(t) and local oscillator generates the carrier signal which is synchronized with the transmitter carrier. Both are applied as I/p to coherent detector which consists of product modulator and LPF.

→ product modulator is used to suppress the carrier from y(t) and LPF is used to remove the interference of noise signal.

→ Decision device based on threshold value it detects the bit whether it is '0' (or) '1'.

→ The channel noisy o/p is given by,

$$y(t) = x(t) + j(t).$$

$$= c(t) \cdot s(t) + j(t) \quad \text{---(1)}$$

$\because x(t) = c(t) \cdot s(t)$

$s(t)$ → binary psk signal.

$c(t)$ → PN signal

$j(t)$ → Interference

In the receiver, the received signal $y(t)$ is multiplied by PN code.

$$u(t) = c(t) \cdot y(t) \quad \text{---(2)}$$

sub. eqn. (1) in (2),

$$= c(t) \cdot [c(t) \cdot s(t) + j(t)]$$

$$= c^2(t)\, s(t) + c(t) \cdot j(t)$$

$c^2(t) = 1$, then $u(t) = s(t) + c(t) \cdot j(t)$ ---(3)

(5) performance parameters of DSSS systems.

(i) processing gain
(ii) probability of error
(iii) Jamming gain.

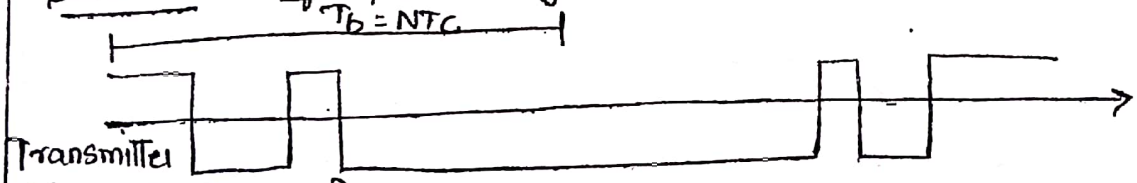
(i) processing gain (PG):

→ is the gain achieved by processing a spread spectrum signal over an unspreaded signal.

→ processing gain is defined as "the ratio of the band width of the spread spectrum signal to the band width of the unspreaded signal.

$$\therefore \text{processing gain} = \frac{\text{BW of spread spectrum signal}}{\text{BW of unspreaded signal}}.$$

Band width of spread signal $m(t)$:



The one bit period of the spread signal $m(t)$ is given by "T_c".

The band width of a NRZ signal is equal to the reciprocal of its one bit period.

$$\therefore \text{BW of spread signal} = \frac{1}{T_c}.$$

Band width of unspread signal:

→ The unspread signal b(t) is an NRZ signal and the B.W of the NRZ signal is reciprocal of the bit period.

∴ B.W. of unspread signal = $1/T_b$.

$$\therefore PG = \frac{1/T_c}{1/T_b} = \frac{T_b}{T_c}$$

(ii) probability of error

$$Pe = \frac{1}{2} \operatorname{erfc} \sqrt{\frac{E_b}{JT_c}}$$

J → Average interference power

E_b → Energy/bit

T_c → chip duration.

$$Pe \downarrow \rightarrow \sqrt{\frac{E_b}{JT_c}} \uparrow$$

(c) Jamming:-

Energy/bit = $E_b = P_s T_b$ P_s → Average sig. power, T_b → bit duration

$$\frac{E_b}{N_0} = \frac{P_s T_b}{N_0}$$

$N_0 = JT_c$; $\frac{E_b}{N_0} = \frac{P_s T_b}{JT_c}$

$$\therefore \frac{E_b}{N_0} = \left(\frac{T_b}{T_c}\right)\left(\frac{P_s}{J}\right)$$

Processing gain $PG = T_b/T_c$

$$\frac{E_b}{N_0} = (PG)\left(\frac{P_s}{J}\right)$$

$$\therefore \frac{J}{P_s} = \frac{PG}{E_b/N_0}$$

Jamming margin

Ps

(6)

Jamming margin is defined as the ratio of average interference power J and the signal power Ps and is expressed in dB as,

(Jamming margin)dB = (processing gain)dB − log log$_{10}$ $\left[\frac{E_b}{N_0}\right]_{min}$

$\left[\frac{E_b}{N_0}\right]_{min}$ → min. bit energy to noise density ratio needed to support the average error probability.

(5) Frequency hopping spread spectrum (FH-SS) signals:

→ The capacity of DSSS s/m to reject jamming is dependent on (PG) processing gain. Under some conditions max. attainable PG is not possible to combat jamming. under such condition alternative system called FH-SS is used.

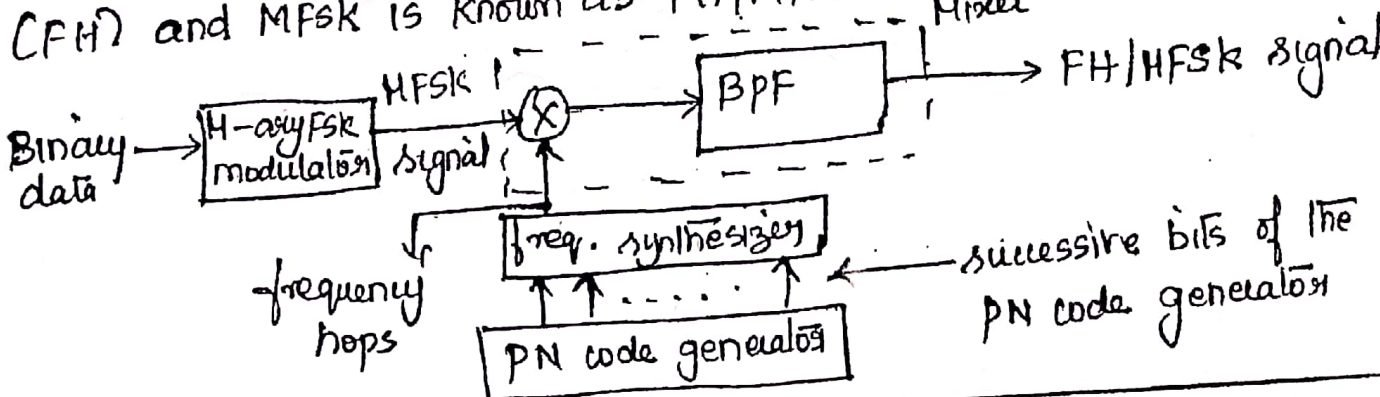
→ Frequency hopping is defined as "the process of randomly hopping the modulated data carrier from one frequency to other". The data is used to modulate a carrier.

→ Depending on the rate of frequency hopping, the FH/MFSK systems are classified in to two categories.

They are, (i) slow frequency hopping
(ii) Fast frequency hopping.

Slow frequency hopping: The symbol Rate (Rs) of the MFSK signal is an integer multiple of the hop rate (Rh). So, several symbols are transmitted corresponding to each frequency hop. So hopping takes place very slowly.

(a) FH/MFSK transmitter: The combination of frequency hopping (FH) and MFSK is known as FH/MFSK.



→ Binary data sequence (b(t)) is applied to M-ary FSK modulator the o/p of which goes to the input of the mixer. The other input to the mixed block is obtained from the digital frequency synthesizer.

→ The mixer consists of a multiplier followed by a band pass filter, which is designed to select the sum frequency component rejecting all other components. This sum component of frequency is then transmitted.

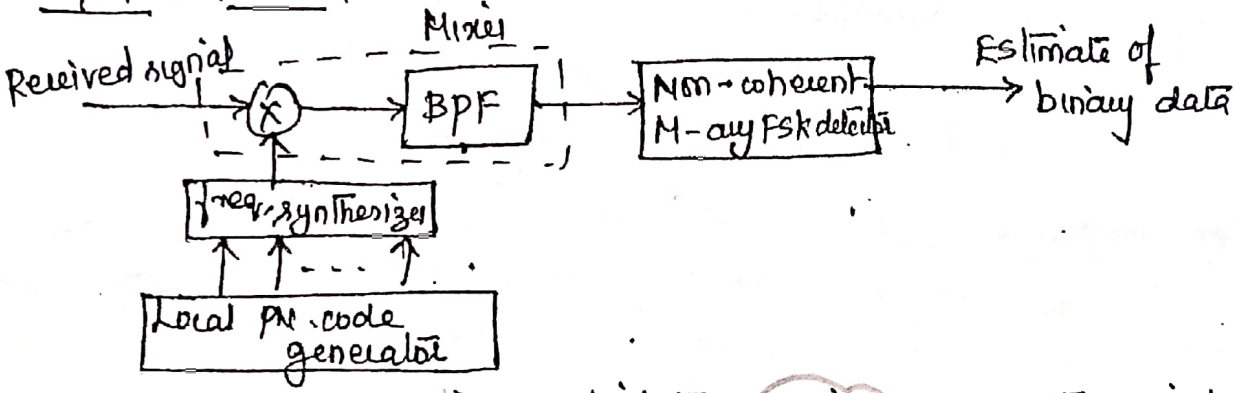
→ M-ary FSK modulator will assign a distinct frequency for each of these M symbols transmitted.

→ The synthesizer o/p at a given instant of time is the freq. hop. Each freq. hop + MFSK signal to produce transmitted signal.

→ o/p of PN generator changes, ∴ synthesizer o/p freq. will change Hence freq. hops produced will vary in a random manner.

→ Total B.W. of FH/MFSK = sum of all freq. hops.

FH/MFSK Receiver.



→ The received signal is applied to a mixer. The other input to the mixer ~~for~~ comes from digital frequency synthesizer.

→ The digital frequency synthesizer is driven by a PN code generator and it is synchronized at the transmitter and generates the same code sequence.

→ So, the frequency hops produced at the synthesizer o/p will be identical to those at the transmitter. At the o/p of multiplier we get I/p signals, their sum and difference.

→ The difference signal is MFSK signal. Thus, the mixer removes the frequency hopping.

→ The MFSK signal at the mixer o/p is then applied to a non coherent MFSK detector and the o/p is digital modulating signal.

chip rate (R_c): $R_c = \max(R_h, R_s)$ R_h → Hop rate
Individual tone of shortest duration is chip rate. R_s → symbol rate

processing gain (PG): $PG = \frac{\text{BW of spread spectrum signal}}{\text{BW of unspread signal}}$

BW of spread spectrum signal:

n → No. bits at the o/p of PN code generator.

2^n → No. of combinations.

2^n → No. of freq. hops.

B.W = $2^n \times f_s$ → symbol freq.

BW of unspread signal (f_s)

$$PG = \frac{2^n f_s}{f_s} = 2^n.$$

Fast Frequency hopping:- The hop rate R_h is an integer multiple of the MFSK symbol rate R_s. so, during the transmission of one symbol the carrier frequency will hop several times. Thus, frequency hopping takes place at a fast rate.

chip Rate R_c = Rate of hopping R_h.

Advantages of FHSS

(i) The synchronization is not greatly dependent on distance.
(ii) High PG than DS-SS system.
(iii) shorter acquisition time makes the s/m faster.

Disadvantage: (i) B.W. is too large.
(ii) complex & expensive freq. synthesizers are used.

⑥ Synchronization in spread spectrum systems:

The code synchronization process in spread spectrum happens in following two phases:

(i) Acquisition and

(ii) Tracking.

→ The acquisition and tracking stages primarily aim to solve the problem of uncertainity of propagation delay between transmitter and Receiver.

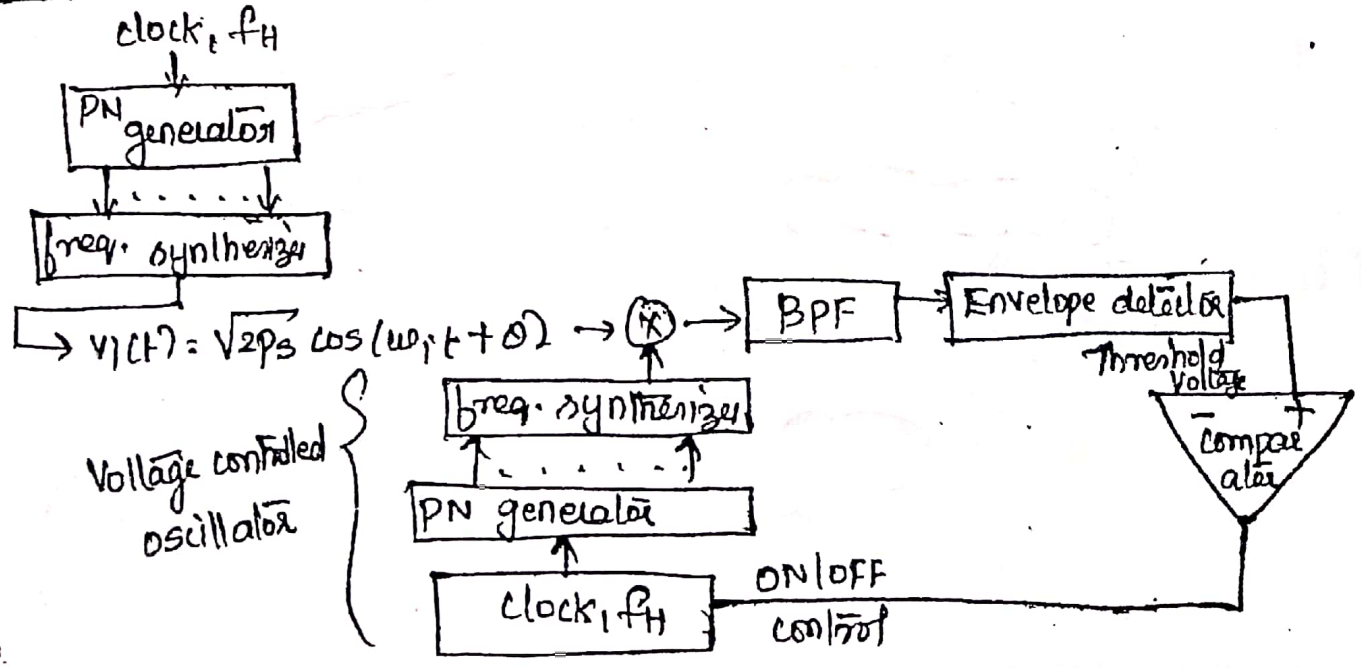
Acquisition: is the coarse code synchronization process. It is the initial phase where the receiver recognizes the transmitter. The objective of this phase is to resolve the code phase errors to within certain bound which can be further reduced by the tracking stage.

Tracking: is also called fine tuning (synchronization). This phase happens upon sucessful acquisition phase.

In the tracking phase, the Tx and Rx need to be in continous synchronization until data transmission is complete.

Tracking continously maintains the best possible waveform fine alignment by means of feed back loop. Thus high PG is achieved (SNR) at the Receiver.

Acquisition (camp and wait) circuit of FH signal:



→ The circuit consists of a mixer (multiplier), a BPF centered at an IF frequency f_0 and having a B.W. equal to twice the hopping rate ($B = 2f_h$), an envelope detector + comparator and voltage controlled oscillator (VCO).

→ VCO consists of a clock, PN generator and frequency synthesizer. The clock is either OFF (or) ON, in which case clock pulses at hopping rate f_h are delivered to the PN generator.

→ PN generator & frequency synthesizer are identical in the Tx & Rx.

→ The freq. synthesizer is merely an oscillator whose ~~out~~ frequency can be controlled by the digital signal applied to it by the PN generator.

→ The detector o/p is compared with a threshold voltage by the comparator which accepts two I/p voltages & provides an o/p which is larger voltage.

→ when detector o/p is less than threshold voltage, then ON/OFF control voltage to the oscillator will ~~be~~ turned off the oscillator.

→ As long as the received frequency is not equal to f_i, the PN generator does not cycle through its states and the receiver synthesizer holds at the frequency $f_0 + f_j$. Thus, the synthesizer remains camped at $f_0 + f_j$. So this is called as camp-and-wait circuit.

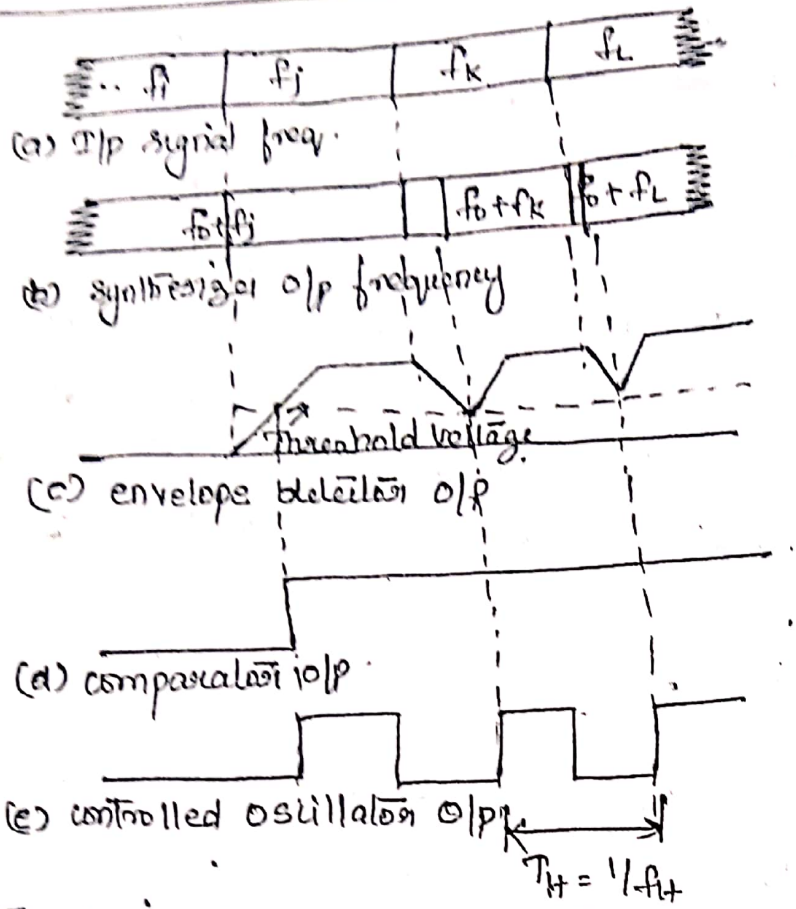
when finally the received signal is f_i,

→ The difference sig. passes through the filter.

→ The detector o/p rises above the threshold.

→ The comparator o/p changes.

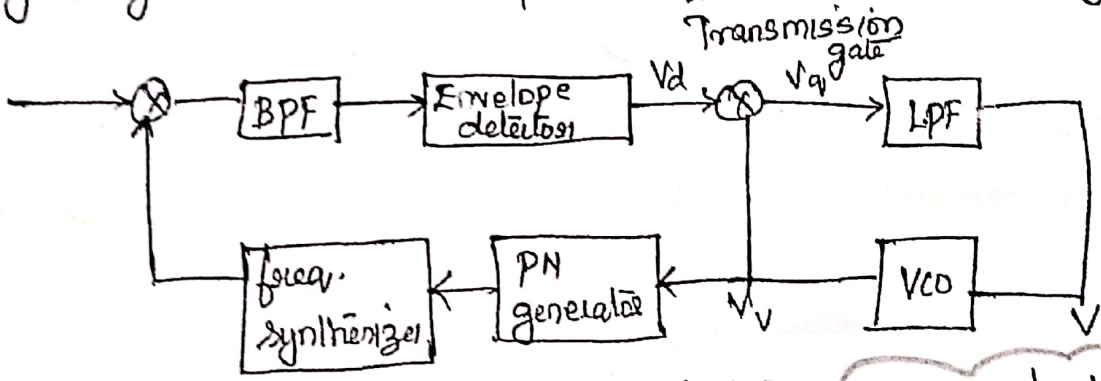
→ The controlled oscillator is turned ON.



waveforms of FH acquisition circuit -

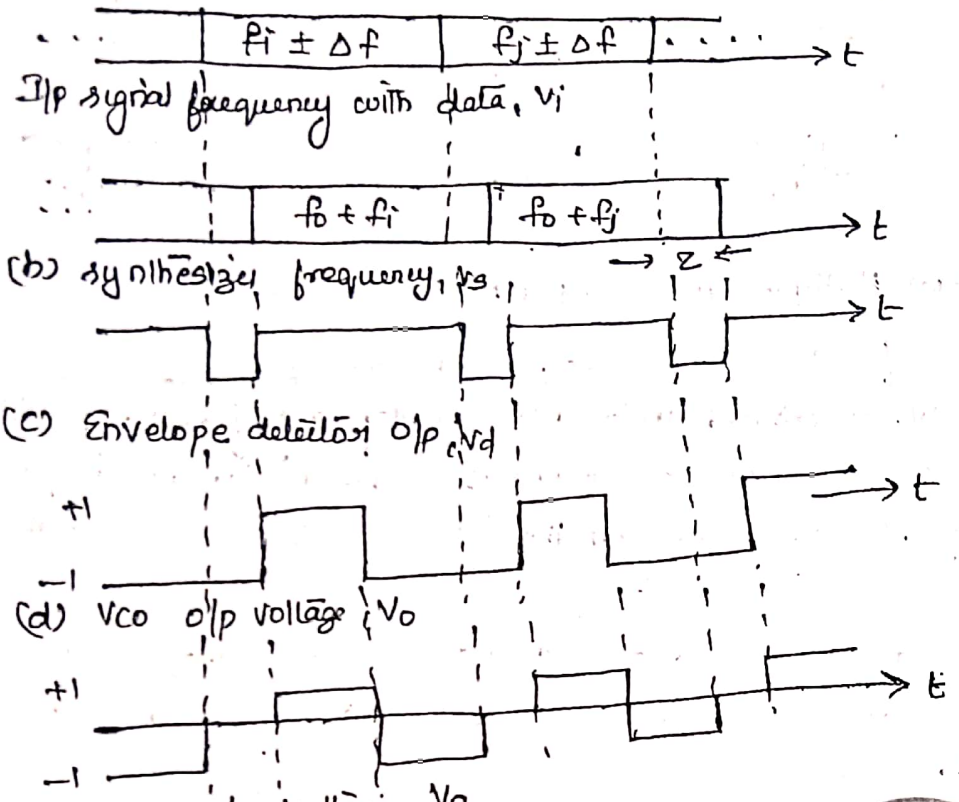
Tracking (Early - Late gate) circuit of FH signal.

→ To effect fine synchronization, we need to replace the VCO clock which can only be turned ON and OFF by VCO and it can be controlled by voltage which measures phase difference b/w two PN generators.



→ The VCO output will be moved between +1V and -1V. The envelope detector o/p responds immediately to the BPF o/p.

→ The gate between envelope detector and LPF is a transmission gate when there is an o/p provided by the envelope detector, the VCO clock is waveform is transmitted through the gate & is not transmitted when detector o/p is zero.



→ The operation of this gate is multiplication process. If ±1V is applied to Vco clock, env detector o/p → 0, when there is no o/p, ~~o/p~~ o/p = 1, when there is an o/p.

→ Depending on whether the receiver PN junction lags (is late) or leads (is early), the control voltage Vc will be of one polarity (or) the other to increase (or) decrease the Vco frequency, moving it always in the direction to reduce z.

→ This fine synchronization scheme, called an early late gate will sustain synchronization even in the presence of disturbances ~~that~~ provided that |z| remains less than T_H.

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(8) Multiple access:

is nothing but two (or) more users simultaneously communicate with each other using the same propagation channel.

Multiple access techniques

- Frequency division multiple access (FDMA)
- Time division multiple access (TDMA)
- code division multiple access (CDMA)
- Space division multiple access (SDMA)

① Frequency Division Multiple access: (FDMA)

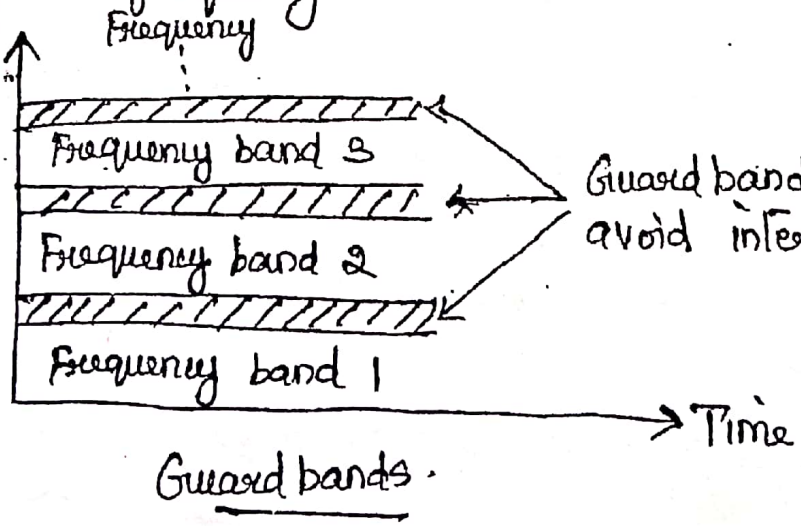
→ FDMA is used for voice and data transmission.

→ The total B.W. is divided in to non-overlapping frequency subbands. Each user is allocated a unique frequency subband (channels) for the duration of the connection, whether the connection is in active (or) idle state.

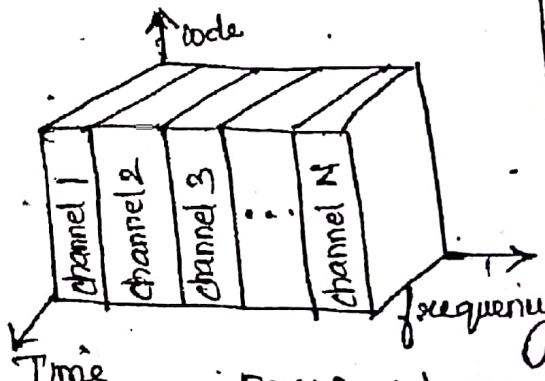
→ These channel are assigned on demand to users who request service. During the period of the call, no other user can share the same channel.

Guard Bands:

The adjacent frequency bands in the FDMA spectrum are likely to interference with each other. Therefore, it is necessary to include the guard bands between the adjacent frequency bands.



Guard bands.



FDHA scheme

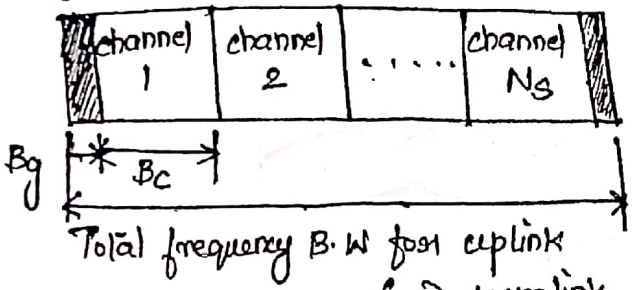
Non-Linear effects in FDMA:

→ In FDMA system, many channel share the same antenna at the base station.

→ The power amplifiers and the power combiners used are non linear, and tend to generate intermodulation frequencies resulting in intermodulation distortion.

→ To minimize the effects of intermodulation distortion, stringent RF filters are required to reject intermodulation distortion. RF filters are heavy and costly.

Number of channels



The no. of channels that can be simultaneously supported in a FDMA system is given by, $N_s = \frac{B_s - 2B_g}{B_c}$

B_s - Total spectrum allocation (or) system B.W

B_g - Guard band allocated at the edge of the allocated spectrum band.

B_c - channel bandwidth.

Spectral Efficiency of FDMA:

$$\eta_{FDMA} = \frac{\text{bandwidth available for data transmission}}{\text{system bandwidth}}$$

No. of data channels in the system = N data = $N_s - N_{ctl}$.

$$\eta_{FDMA} = \frac{N_{data} B_c}{B_s} < 1$$

N_{CH} : No. of allocated control channels.
N_S = Total No. of available channel in the system.

Advantages :

(i) FDMA is relatively simple to implement.
(ii) is implemented in narrow band systems.
(iii) The complexity of FDMA mobile system is lower when compared to TDMA systems;
(iv) Absence of synchronization.
(v) To provide interference - free transmissions between uplink and downlink channels, the frequency allocations have to be seperated by guard bands.

Disadvantages:

(i) This type of multiple access support is narrow band, and is not suitable for multimedia communications with various transmission rates.
(ii) If an FDMA channel is not in use, it cannot be used by other users to increase (or) share capacity. It is a wasted Resource.
(iii) Lack of flexibility in case of reconfiguration.
(iv) Have higher cell site system costs as compared to TDMA.
(v) To minimize the effects of intermodulation distortion, and adjacent channel interference, stringent RF filters are required.

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(2) Time division multiple access:

→ divides the radio spectrum in to time slots, and in each slot only one user is allowed to either transmit (or) receive.
→ In TDMA, channel time is partitioned in to frames. Every user in service has an opportunity to transmit one frame.
→ To achieve this, TDMA frame is further partitioned in to time slots. users have to transmit slots from frame to frame.